SEMESTER END EXAMINATION APRIL-MAY, 2026

Course Name: - B.Tech **Semester:-** IV

Paper Name: - COMPUTER ARCHITECTURE **Paper Code:-** NES-404

Time - 3 Hrs + 20 minutes per hour extra time for V.I. & examinees with writer. **Max Marks-70**

Instructions:

- The question paper consists of three sections namely A, B, C. All sections are compulsory.
- Section A- Each question carries **3 mark. All questions are compulsory.**
- Section B- Answer any **5 out of 7** given questions. Each question carries **7 marks.**
- Section C- Answer any **2 out of 3** given questions. Each question carries **10 marks.**

Section – A

Multiple Choice Questions

1. Answer all the following questions. **5x3 =15**

i) Which of the following is NOT a functional unit of a computer?
A) ALU
B) Control Unit
C) Compiler
D) Memory Unit

ii) IEEE 754 standard is related to:
A) Integer arithmetic
B) Floating-point arithmetic
C) Boolean algebra
D) Memory management

iii) Cache memory is used to:
A) Store permanent data
B) Increase processing speed
C) Store input data
D) Replace RAM

iv) Pipelining is used to:
A) Reduce memory size
B) Execute multiple instructions simultaneously
C) Store data permanently
D) Improve I/O speed

v) Instruction format mainly consists of:
A) Opcode only
B) Operand only
C) Opcode + Operand(s)
D) Address only

Scanned with OKEN Scanner

Section – B
Short Answer Questions

2. Answer any five of the following questions. **5x7=35**

i) Explain the basic structure of a computer with a neat diagram. Describe the functions of each unit (ALU, Control Unit, Memory, Input/Output).

ii) What is Floating Point Arithmetic? Explain the IEEE 754 standard representation of floating-point numbers.

iii) Compare Hardwired Control Unit and Microprogrammed Control Unit. Discuss their advantages and disadvantages.

iv) Explain different types of adders used in digital systems. Describe the working of Parallel Adder and Carry Look-Ahead Adder with logic diagrams.

v) Explain pipelining in computer architecture. Discuss its working, advantages & limitations.

vi) Explain the bus structure of a processor. How are data, address, and control buses used in instruction execution?

vii) Explain the general organization of a processor with a neat block diagram.

Section – C
Descriptive Questions

3. Answer any two of the following question. **2x10=20**

i) What is an instruction format? Explain different types of instructions and addressing modes with examples.

ii) Describe the memory hierarchy with a diagram. Explain the working of cache memory and Main memory.

iii) Explain different types of multipliers in computer architecture. Describe Array Multiplier and Booth's Multiplier algorithm in detail.

****

Scanned with OKEN Scanner